PICOSCALE Controller GPIO interface description and Breakout Box

The **PICO**SCALE controller provides several high performance general purpose inputs and outputs (GPIOs) via a D-Sub 44 HD interface. This interface can be most conveniently accessed via the **PICO**SCALE *Breakout Box*. Alternatively, the user can also connect self-made periphery to the connector.

> We strongly recommend the use of the *Breakout Box* as it contains several buffers and other measures to prevent the **PICO**SCALE Controller from possible damages due to accidentally high voltages, for example.

1. BREAKOUT BOX

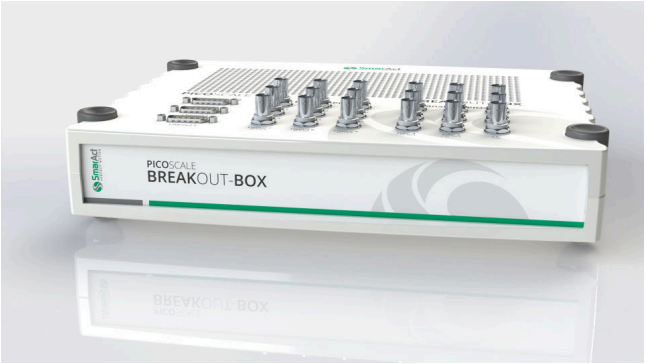

Figure 1. **PICO**SCALE *Breakout Box*

In order to achieve the full performance of the **PICO**SCALE GPIO interface, we strongly recommend to use the **PICO**SCALE *Breakout Box* (BOB), cf. Figure 1. Using BOB guarantees appropriate signal conditioning (unified voltage levels), signal buffering and convenient access to the signals via BNC connectors. Furthermore, all BNC connectors are equipped with an ESD and over-voltage protection. This prevents damage to the **PICO**SCALE controller in case wrong voltages are inadvertently applied to the input pins.

Table 1. *Key features of Breakout Box*

Parameter	Typical Value
Chassis dimension	33 x 27 x 7.3 cm^3
Weight	2.75 kg

1.1 Differential Digital Interface DDI

The Differential Digital Interface (DDI) provides differential digital signals, which can be used for different digital protocols, e.g. AquadB and Serial Data. With the *Breakout Box* the signals are distributed to three DSub 15 connectors, one per channel. The pin assignment is shown in Figure 2 and specified in Table 2. For the precise usage and configuration possibilities, please refer to the **PICO**SCALE User Manual.

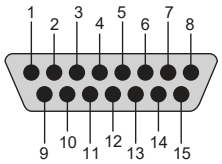

Figure 2. *Pin assignment of the DSub 15 connector.*

Table 2. *Pin assignment of DSub 15 connectors*

Signal	Direction	AquadB	serial data
1	Out	A positive	CLOCK positive
2	Out	B positive	DATA positive
3 - 7	-	not connected	-
8	-	System Ground	System Ground
9	Out	A negative	CLOCK negative
10	Out	B negative	DATA negative
11 - 15	-	not connected	-
Shielding	-	System Ground	System Ground

Main performance parameters are listed in Table 3.

Table 3. *Output and input voltages, and bandwidth of the DSub15 connector.*

Parameter	Typical Value
Diff. output voltage	0 - 5 V
Diff. high-level input voltage	0.2 V
Diff. low-level input voltage	-0.2 V
Max. frequency per pair	5 MHz

1.2 BOB digital GPIOs

The digital GPIOs are buffered on the *Breakout Box*. The signals labelled with Digital1 - Digital4 have a 5 V high level, while the Digital5 - Digital9 signals have a 3.3 V high level. All digital GPIOs are matched with a 50 Ω serial resistor. The direction of the buffers is automatically set with the direction of the digital GPIOs within the **PICO**SCALE Controller. Main performance parameters are listed in Table 4 (for the Digital 1-4 signals) and Table 5 (for the Digital 5-9 signals).

Table 4. *Main performance data BOB Digital 1-4 GPIO Buffer*

Parameter	Typical Value
Digital 1-4 output	0 - 5 V
High-level input	3.5 V
Low-level input	1.5 V
Switching time	≦ 50 ns

Table 5. *Main performance data BOB Digital 5-9 GPIO Buffer*

Parameter	Typical Value
Digital 5-9 output	0 - 3.3 V
High-level input	2 V
Low-level input	0.8 V
Switching time	≦ 50 ns

Due to the limited bandwidth it is recommended to use the digital GPIOs with a maximum frequency of 1 MHz. Using higher frequencies may cause asymmetries in the duty cycle of the signal. Depending on the cable connected to the BNC connector the digital GPIOs can over-/undershoot with up to 1 V. The best signal form can be achieved in a 50 Ω environment and with short cable lengths.

1.3 BOB analog GPIOs

The *Breakout Box* buffers and converts the analog in- and outputs to single-ended signals with an amplitude of ±10 V.

1.3.1 ADCs

For an exact mapping of voltage to ADC resolution it is recommended to do a calibration of the ADC input (with the **PICO**SCALE *Calculation System*, for example). The input impedance of the ADC1 input is approximately 2.4 kΩ. The input impedance of ADC2 and ADC3 is approximately 24 kΩ. For a performance overview see table 6 and 7.

Table 6. *Main performance data of ADC1*

Parameter	Typical Value
Full-scale input voltage	± 10 V
Sample-rate	10 MS /s
Resolution	16 Bit
Bandwidth f_{1dB}	2-2.5 MHz
Impedance	2.4 kΩ

Table 7. *Main performance data of ADC2 and ADC3*

Parameter	Typical Value
Full-scale input voltage	± 10 V
Sample-rate	100 kS /s
Resolution	16 Bit
Bandwidth f_{1dB}	35-45 kHz
Impedance	24 kΩ

1.3.2 DACs

The digital-to-analog converters (DACs) have a maximum output voltage of ±10 V output signal (single ended). The output of DAC1 can drive currents up to 35 mA with a capacitive load up to 33 pF. DAC2-DAC5 are the **PICO**SCALE DAC can drive currents up to ±30 mA with a capacitive load of up to 200 pF. However, if several channels are connected simultaneously, the maximum current is reduced. For a performance overview see table 12 and 13.

Table 8. *Main performance data of DAC1*

Parameter	Typical Value
Full-scale output voltage	± 10 V
Sample-rate	10 MS /s
Resolution	12 Bit
Bandwidth f_{1dB}	2-2.5 MHz

2. HANDLING INSTRUCTIONS WITHOUT BREAKOUT BOX

When the **PICO**SCALE *Breakout Box* is not used, please consider the following descriptions to ensure secure handling. The schematic and pinout of the D-Sub 44HD interface is provided in section 3.

Table 9. *Main performance data of DAC2-5*

Parameter	Typical Value
Full-scale output voltage	± 10 V
Sample-rate	200 kS /s
Resolution	16 Bit
Bandwidth f_{1dB}	130-170 kHz

2.1 DDI

The DD (digital differential) interface of the **PICO**SCALE controller is a four-wire interface with two differential quadrature signals, transmitted by an RS485 transceiver (LTC1685). The output signals of one differential quadrature pair is shown schematically in figure 3.

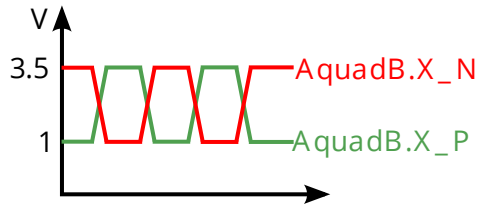

Figure 3. *AquadB differential output signal.*

The **PICO**SCALE controller provides its differential quadrature signals according to industry standard AquadB receivers. Occasionally, it might be necessary to convert the data to a single ended signal and/or to match the signal levels. In this case it is recommended to do the signal conversion close to the receiver, in order to keep the advantage of differential data transmission.

2.2 Digital IO interface

The D-Sub 44HD connector allows access to nine digital IOs (GPIO.TTL* and GPIO.CMOS*, see table 14). The signal GPIO.1WireCom is reserved for the communication of the **PICO**SCALE controller with the Breakout-Box and cannot be used for general purpose. All other digital IOs are Low Voltage CMOS (LVC) signals with a range from 0 V to 3.3 V [1] The edge steepness of the signals strongly depends on the connected load. Therefore we recommend to externally buffer the digital IOs. With a proper setup, clock frequencies of up to 10 MHz can be reached. The direction of the IOs can be configured by the **PICO**SCALE Control GUI or by corresponding API commands.

2.3 General purpose ADCs

The **PICO**SCALE controller provides three ADCs with 16 bit resolution. ADC1 (GPIO.ADC1_P and GPIO.ADC1_N in 14) has a sample-rate of 10 MHz and a differential input, as shown in table 10.

Table 10. *Main performance data of ADC1*

Parameter	Typ. value
Full-scale input voltage (differential)	2 $V_{PP_{diff}}$
Input common mode voltage	2.5 V
Sample-rate	10 MS /s
Resolution	16 Bit
Bandwidth	2.5 MHz

Figure 4 shows the input signal setting to reach full-scale modulation of ADC1 with a differential signal. Transmitting data via a differential input is advantageous since it is insensitive to external distortions. This type of transmission is therefore recommended.

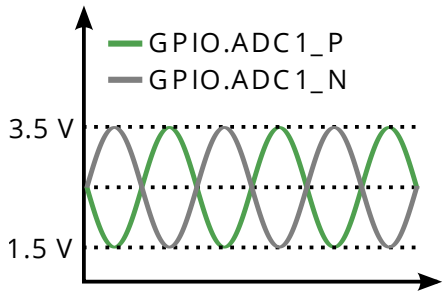

Figure 4. *ADC1 differential input signal setting for FSR modulation.*

For a single ended configuration the negative input (GPIO.ADC1_N) can be connected to a constant voltage of 2.5 V and the amplitude of the positive input can be doubled.
ADC2 and ADC3 have sample-rates of 100 kHz and single-ended inputs. As shown in table 11, the analog bandwidth is larger than the half sample-rate of the ADCs. Thus, it is possible to read in frequencies up to 50 kHz without attenuation. Nevertheless, it is strongly recommended to add a low pass filter at the input of the ADCs to reduce aliasing effects.

2.4 General purpose DACs

The **PICO**SCALE controller provides five analog DAC outputs. DAC1 is a fast sampling DAC with a resolution of 12 bit. The analog bandwidth is limited to 2.5 MHz. It has a differential output which is more robust against distortions.
DAC2-5 have slower sampling-rates of 200 kHz, but resolutions of 16 bit, as shown in table 13. Passive low pass filters at the output of DAC2-5 reduce the analog

[1] For **PICO**SCALE controllers with product codes PSC-CTRL-V1.0-TAB and PSC-CTRL-V1.1-TAB the signals GPIO.TTL* have a range of [0, 5] V and a serial termination resistor of 100 Ω.

Table 11. *Main performance data of ADC2 and ADC3.*

Parameter	Typ. value	Unit
Full-scale input voltage (single ended)	3.3	V_{PP}
Input common mode voltage	1.5	V
Sample-rate	100	kS /s
Resolution	16	Bit

Table 12. *Main performance data of DAC1.*

Parameter	Typ. value	Comment
Full-scale output voltage	9 V	differential output voltage (peak-to-peak)
output common mode voltage	0 V	
Sample-rate	10 MS /s	
Resolution	12 Bit	
Bandwidth	2.5 MHz	

Table 13. *Main performance data of DAC2-5.*

Parameter	Typ. value	Comment
Full-scale output voltage	5 V	single ended output voltage (peak-to-peak)
output common mode voltage	2.5 V	
Sample-rate	200 kS /s	
Resolution	16 Bit	
Bandwidth	200 kHz	

bandwidth to approx. 200 kHz. Each filter has a series resistor of 1.2 kΩ which leads to a voltage drop while loading the output. In this case it is recommended to buffer the output of DAC2-5.

2.5 Power supply +12 V

The 12 V power supply can be used to drive additional circuitry. Since the voltage can vary by several percent, it is not recommended to use it as direct source for an analog stage, but as a supply for a LDO. The maximum current is limited to 250 mA.

3. PINOUT OF THE D-SUB 44HD

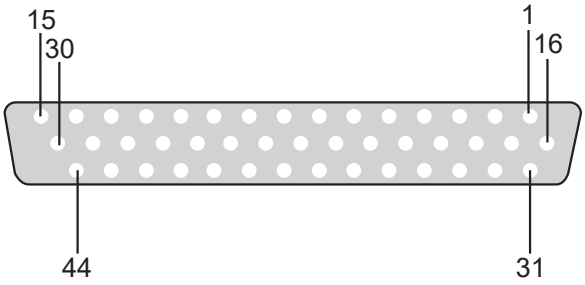

Figure 5. *Schematic of a female D-Sub 44HD.*

Table 14. *Pin description of the D-Sub 44HD connector with GPIO and AquadB interfaces.*

Pin	Signal	Direction	Function
1	AquadB.1A_N	Out	Ch 1 AquadB differential pair A negative
2	AquadB.1B_N	Out	Ch 1 AquadB differential pair B negative
3	AquadB.2B_P	Out	Ch 2 AquadB differential pair B positive
4	AquadB.2B_N	Out	Ch 2 AquadB differential pair B negative
5	GND	-	System Ground
6	AquadB.3A_P	Out	Ch 3 AquadB differential pair A positive
7	AquadB.3A_N	Out	Ch 3 AquadB differential pair A negative
8	AquadB.3B_P	Out	Ch 3 AquadB differential pair B positive
9	AquadB.3B_N	Out	Ch 3 AquadB differential pair B negative
10	GND	-	System Ground
11	NC	-	not connected
12	GPIO.ADC3	In	GPIO ADC
13	GPIO.ADC2	In	GPIO ADC
14	GPIO.DAC2	Out	GPIO DAC
15	GPIO.DAC5	Out	GPIO DAC
16	AquadB.1A_P	Out	Ch 1 AquadB differential pair A positive
17	AquadB.1B_P	Out	Ch 1 AquadB differential pair B positive
18	GND	-	System Ground
19	AquadB.2A_P	Out	Ch 2 AquadB differential pair A positive
20	AquadB.2A_N	Out	Ch 2 AquadB differential pair A negative
21	GPIO.CMOS2 (Dig. 6)	Bi	Digital GPIO (Low Voltage CMOS (LVC) 3.3V)
22	GPIO.CMOS3 (Dig. 7)	Bi	Digital GPIO (LVC 3.3V)
23	GPIO.CMOS4 (Dig. 8)	Bi	Digital GPIO (LVC 3.3V)
24	GND	-	System Ground
25–26	NC	-	not connected
27	GPIO.DAC1_N	Out	GPIO differential DAC negative
28	GPIO.ADC1_P	In	GPIO differential ADC positive
29	GPIO.DAC3	Out	GPIO DAC
30	GPIO.DAC4	Out	GPIO DAC
31	GPIO.TTL1 (Dig. 1)	Bi	Digital GPIO (LVC 3.3V)
32	GPIO.TTL2 (Dig. 2)	Bi	Digital GPIO (LVC 3.3V)
33	GPIO.TTL4 (Dig. 4)	Bi	Digital GPIO (LVC 3.3V)
34	GPIO.TTL3 (Dig. 3)	Bi	Digital GPIO (LVC 3.3V)
35	GPIO.CMOS5 (Dig. 9)	Bi	Digital GPIO (LVC 3.3V)
36	GPIO.1WireCom	Bi	BOB communication line, do not use
37	GPIO.CMOS1 (Dig. 5)	Bi	Digital GPIO (LVC 3.3V)
38	GND	-	System Ground
39–41	NC	-	not connected
42	GPIO.DAC1_P	Out	GPIO differential DAC positive
43	GPIO.ADC1_N	In	GPIO differential ADC negative
44	SUP.+12V	Out	Power supply; 12 V - 10 V max. current 250 mA
Shielding	GND	-	System Ground

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